REMARKS

Claims 1 – 21 and 32 - 47 are pending in the present application, wherein claims 46 and 47 are newly added.

On 2 MAY 2006, Applicant and Examiner Luu held a teleconference. Applicant thanks Examiner Luu for making time for the teleconference.

On 19 JAN 2005, Applicant submitted a first information disclosure statement (IDS), which included a copy of a German-language reference, namely DE 37 44 128. On 17 MAR 2005, Applicant submitted a second IDS, which included an English translation of DE 37 44 128. Section 1 of the Office Action indicates that the English translation is missing from the second IDS. Accordingly, Applicant is submitting herewith, another copy of the English translation of DE 37 44 128, and respectfully request that the in the next communication, the Examiner **acknowledge consideration of the English translation of DE 37 44 128.**

The Office Action, section 2, is requiring a new title of the invention. However, in an office action dated 19 OCT 2005, the Examiner required a new title of the invention, and on 19 JAN 2006, Applicant submitted an amendment in which Applicant amended the title to read "Apparatus For Accessing An Active Pixel Sensor Array". Applicant believes that the title submitted on 19 JAN 2006 is adequately descriptive of the invention, and therefore suspects that the Examiner may not have noticed the amended title of 19 JAN 2006. In order to ensure that there is no confusion, **Applicant is requesting** that if the Examiner still believes that the title of 19 JAN 2006 is not descriptive, that the Examiner please affirmatively refer to the title of 19 JAN 2006 as being non-descriptive.

In section 4 of the Office Action, claims 1, 2, 4 – 9, 11, 13, 14, 16 – 23 and 25 – 30 are rejected under 35 U.S.C. 102(b), as being anticipated by U.S. Patent No. 5,262,871 to Wilder et al. (hereinafter "the Wilder et al. patent"). Claims 22, 23 and 25 – 30 are canceled. Of the claims in this rejection that

that are still pending, two are independent, namely claims 1 and 11. In the present response, Applicant is clarifying an aspect of claims 1 and 11 that is neither disclosed nor suggested by the art of record.

Claim 1 provides for a circuit. The circuit includes a decoder for receiving a memory address within a memory address space of a processor, and converting the memory address into a row address and a column address that designate a position of a pixel in an active pixel sensor array.

The Wilder et al. patent, in FIG. 1, discloses a system that includes a row decoder 12, a column decoder 14, an image sensor 10, and a processor/computer 18. Processor/computer 18 produces supervisory signals that are applied to row decoder 12 and column decoder 14 (col. 4, lines 54 – 56). The supervisory signals include address signals (col. 5, lines 2 – 3), and more particularly, as shown in FIG. 2, the address signals include a row address that is presented to row decoder 12, and a column address that is presented to column decoder 14. Thus, as shown in FIG. 2, row decoder 12 receives a row address, and column decoder 14 receives a column address.

The Office Action suggests that row decoder 12 and column decoder 14 of the Wilder et al. patent are descriptive of the decoder of claim 1. However, whereas row decoder 12 and column decoder 14 receive <u>a row address and a column address</u>, respectively, they do not receive <u>a memory address within a memory address space of a processor</u>, as does the decoder of claim 1.

Moreover, whereas row decoder 12 and column decoder 14 <u>receive a row address and a column address</u>, respectively, they do not <u>convert</u> a memory address <u>into a row address and a column address</u>, as does the decoder of claim 1.

Consequently, the Wilder et al. patent does not disclose a decoder for **receiving a memory address** within a memory address space of a processor, and **converting** the memory address **into a row address and a column address** that designate a position of a pixel in an active pixel sensor array, as recited in claim 1.

As noted above, in the Wilder et al. patent, processor/computer 18 patent produces supervisory signals that include a row address and a column address. However, the Wilder et al. patent does not describe processor/computer 18 as receiving a memory address within a memory address space of a processor. Moreover, as processor/computer 18 is apparently executing a program (see col. 18, line 4), it would be a generator of a memory address (within its own memory address space) rather than a receiver of the memory address. Thus, processor/computer 18 is neither descriptive nor suggestive of a decoder for **receiving a memory address within a memory address space of a processor**, as recited in claim 1.

Additionally, one of the benefits provided by the decoder of claim 1 is that since the decoder is for receiving a memory address within a memory address space of a processor, and converting the memory address into a row address and a column address that designate a position of a pixel in an active pixel sensor array, in a case where the decoder is used in cooperation with a microprocessor, the decoder relieves the microprocessor of the burden of having to perform the conversion. **The Wilder et al. patent does not suggest such a benefit.**

Applicant submits that for the several reasons provided above, the Wilder et al. patent does not anticipate claim 1.

Claims 2 and 4 – 9 depend from claim 1. By virtue of this dependence, claims 2 and 4 – 9 are also novel over the Wilder et al. patent.

Claim 11 includes recitals similar to those of claim 1, as described above. As such, claim 11, for reasoning similar to that provided in support of claim 1, is also novel over the Wilder et al. patent.

Claims 13, 14 and 16 – 21 depend from claim 11. By virtue of this dependence, claims 13, 14 and 16 – 21 are also novel over the Wilder et al. patent.

As mentioned above, claims 22, 23 and 25 – 30 are canceled. As such, the rejection of claims 22, 23 and 25 – 30 is rendered moot.

Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1, 2, 4 – 9, 11, 13, 14, 16 – 23 and 25 – 30, as set forth in section 4 of the Office Action.

In section 5 of the Office Action, claims 22 and 26 – 29 are rejected. However, claims 22 and 26 – 29 are canceled. Withdrawal of the rejection set forth in section 5 of the Office Action is respectfully solicited.

In section 6 of the Office Action, claims 22 and 25 – 29 are rejected. Claims 22 and 25 – 29 are canceled. Withdrawal of the rejection set forth in section 6 of the Office Action is respectfully solicited.

In section 8 of the Office Action, claims 24 and 25 are rejected. Claims 24 and 25 are canceled. Withdrawal of the rejection set forth in section 8 of the Office Action is respectfully solicited.

In section 9 of the Office Action, claims 3, 12, 15, 32 – 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent in view of U.S. Patent No. 6,512,218 to Canini et al. (hereinafter "the Canini et al. patent").

Claim 3 depends from claim 1, and claims 12 and 15 depend from claim 11. The Office Action introduces the Canini et al. patent with a suggestion that the Canini et al. patent discloses an A/D converter for representing a charge read from a pixel as a digital value. Applicant submits that the Canini et al. patent does not make up for the deficiencies of the Wilder et al. patent as the Wilder et al. patent relates to claims 1 and 11. Accordingly, Applicant further submits that claims 1 and 11, and therefore claims 3, 12 and 15, by virtue of their dependencies, are all patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Claim 32 is an independent claim. In the present response, Applicant is clarifying an aspect of claim 32 that is neither disclosed nor suggested by the art of record.

Claim 32 provides for a system. The system includes a decoder, similar that of claim 1, as described above, for receiving a memory address, and converting the memory address into a row address and a column address that designate a position of a pixel in an active pixel sensor array. The system further includes a microprocessor for providing the memory address, and the memory address is within a memory address space of the microprocessor.

As mentioned above, in the Wilder et al. patent processor/computer 18 produces supervisory signals that include a row address and a column address, which are received by row decoder 12 and column decoder 14, respectively. Thus, processor/computer 18 does not provide a memory address within a memory address space of processor/computer 18 to row decoder 12 and column decoder 14, and row decoder 12 and column decoder 14 do not receive a memory address within a memory address space of processor/computer 18. The Canini et al. patent does not make up for this deficiency. Consequently, the cited combination of the Wilder et al. and Canini et al. patents does not disclose or suggest **a microprocessor for providing a memory address within a memory address space of the microprocessor, and a decoder for receiving the memory address,** as recited in claim 32. Accordingly, claim 32 is patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Claims 33 – 39 and 42 depend from claim 32. By virtue of this dependence, claims 33 – 39 and 42 are also patentable over the cited combination of the Wilder et al. and Canini et al. patents.

Applicant respectfully requests reconsideration and withdrawal of rejection of claims 3, 12, 15, 32 – 39 and 42, as set forth in section 9 of the Office Action.

In section 10 of the Office Action, claims 10 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent in view of U.S. Patent No. 5,296,852 to Rathi (hereinafter "the Rathi patent").

Claim 10 depends from claim 1. The Office Action introduces the Rathi patent with a suggestion that the Rathi patent discloses summing pixel values. Applicant submits that the Rathi patent does not make up for the deficiencies of the Wilder et al. patent as the Wilder et al. patent relates to claim 1. Accordingly, Applicant submits that claim 1, and claim 10, by virtue of its dependence on claim 1, are both patentable over the cited combination of the Wilder et al. and Rathi patents.

Claim 31 is canceled. Thus, the rejection of claim 31 is rendered moot.

Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 10 and 31, as set forth in section 10 of the Office Action.

In section 11 of the Office Action, claims 41 and 43 – 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wilder et al. patent in view of the Canini et al. patent and U.S. Patent No. 6,825,936 to Metcalfe et al. (hereinafter "the Metcalfe et al. patent").

Claims 41 and 43 – 45 depend from claim 32. Above, Applicant explained that claim 32 is patentable over the cited combination of the Wilder et al. and Canini et al. patents. The Office Action introduces the Metcalfe et al. patent with a suggestion that the Metcalfe et al. patent teaches sub-frames of pixels having different integration times. Applicant submits that the Metcalfe et al. patent does not make up for the deficiencies of the Wilder et al. and Canini et al. patents, as the Wilder et al. and Canini et al. patents relate to claim 32. Accordingly, Applicant submits that claim 32, and claims 41 and 43 – 45, by virtue of their dependence on claim 32, are all patentable over the cited combination of the Wilder et al., Canini et al, and Metcalfe et al. patents.

Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 41 and 43 – 45, as set forth in section 11 of the Office Action.

As mentioned above, Applicant is clarifying an aspect of claims 1, 11 and 32 that is neither disclosed nor suggested by the art of record. Applicant is also amending claim 1 to remove recitals that do not appear to be necessary for patentability. Applicant is amending claims 2, 14 and 34 for consistency with the clarification of claims 1, 11 and 32, and amending claim 15 to correct a grammatical error. None of the amendments is intended to narrow the meaning of any term of the claims, and as such, the doctrine of equivalents should be available for all of the elements of all of the claims.

Applicant is adding claims 46 and 47 to preserve features that were previously presented in claim 1.

In view of the foregoing, Applicant respectfully submits that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicant respectfully requests favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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